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Hiroki SHINKAWATA)

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For: SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE MANUFACTURING METHOD)

VERIFICATION OF TRANSLATION

Honorable Commissioner of
Patents and Trademarks
Washington D.C. 20231

Sir:

Yasuyo Moriguchi residing at c/o Yoshida, Yoshitake and Arita Patent Office of Sumitomo-Seimei OBP Plaza Building, 4-70, Shiromi 1-chome, Chuo-ku, Osaka, Japan declares:

1) that I know well both the Japanese and English languages;

2) that I translated the priority documents of the Japanese Patent Application No. 2003-044155 from Japanese to English;

3) that the attached English translation is a true and correct translation of the priority documents of the Japanese Patent Application No. 2003-044155 to the best of my knowledge and belief; and

4) that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: January 19, 2006

Signature: Yasuyo Moriguchi
Yasuyo MORIGUCHI

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Applicant(s): **MITSUBISHI DENKI KABUSHIKI KAISHA**

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【Inventor】
【Domicile】 c/o Mitsubishi Denki Kabushiki Kaisha, 2-3 Marunouchi 2-chome, Chiyoda-ku, TOKYO 100-8310 JAPAN
【Name】 Hiroki SHINKAWATA
【Applicant of Patent Application】
【Identification Number】 000006013
【Name】 MITSUBISHI DENKI KABUSHIKI KAISHA
【Attorney】
【Identification Number】 100089233
【Patent Attorney】
【Name】 Shigeaki YOSHIDA
【Attorney】
【Identification Number】 100088672
【Patent Attorney】
【Name】 Hidetoshi YOSHITAKE
【Attorney】
【Identification Number】 100088845
【Patent Attorney】
【Name】 Takahiro ARITA
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【 Title of the Invention 】 Semiconductor Device and Semiconductor Device Manufacturing Method

【Claims】

【Claim 1】 A semiconductor device comprising:

a semiconductor substrate having a memory formation region in which a memory device is formed and a logic formation region in which a logic device is formed;

a first impurity region formed in an upper surface of said semiconductor substrate in said memory formation region;

a second impurity region formed in the upper surface of said semiconductor substrate in said logic formation region;

a third impurity region formed in an upper surface of said first impurity region and having a conductivity type different from that of said first impurity region;

a fourth impurity region formed in an upper surface of said second impurity region and having a conductivity type different from that of said second impurity region;

a first silicide film formed in an upper surface of said third impurity region;

a capacitor formed above said first silicide film and electrically connected to said first silicide film; and

a second silicide film formed in an upper surface of said fourth impurity region and having a larger thickness than said first silicide film.

【Claim 2】 The semiconductor device according to claim 1, wherein said fourth impurity region is a source/drain region of a MOS transistor.

【Claim 3】 The semiconductor device according to either of claim 1 or 2, further comprising,

first and second gate structures each formed on the upper surface of said

semiconductor substrate in said memory formation region and spaced apart at a given distance from each other, and

third and fourth gate structures each formed on the upper surface of said semiconductor substrate in said logic formation region and spaced apart at a given distance from each other,

wherein said first and second silicide films are provided between said first and second gate structures and between said third and fourth gate structures, respectively, and

a first gate aspect ratio that is defined by the distance between said first and second gate structures and a height of said first and second gate structures is larger than a second gate aspect ratio that is defined by the distance between said third and fourth gate structures and a height of said third and fourth gate structures.

【Claim 4】 The semiconductor device according to claim 3, wherein said first gate aspect ratio is larger than 0.8.

【Claim 5】 The semiconductor device according to claim 1, further comprising,

a fifth impurity region formed in the upper surface of said semiconductor substrate in said logic formation region,

a sixth impurity region formed in an upper surface of said fifth impurity region and having a conductivity type different from that of said fifth impurity region, and

a third silicide film formed in an upper surface of said sixth impurity region and having a larger thickness than said first and second silicide films.

【Claim 6】 The semiconductor device according to claim 5, wherein each of said fourth and sixth impurity regions is a source/drain region of a MOS transistor.

【Claim 7】 The semiconductor device according to either of claim 5 or 6, further comprising,

first and second gate structures each formed on the upper surface of said semiconductor substrate in said memory formation region and spaced apart at a given distance from each other,

third and fourth gate structures each formed on the upper surface of said semiconductor substrate in said logic formation region and spaced apart at a given distance from each other, and

fifth and sixth gate structures each formed on the upper surface of said semiconductor substrate in said logic formation region and spaced apart at a given distance from each other,

wherein said first to third silicide films are provided between said first and second gate structures, between said third and fourth gate structures, and between said fifth and sixth gate structures, respectively,

a first gate aspect ratio that is defined by the distance between said first and second gate structures and a height of said first and second gate structures is larger than a second gate aspect ratio that is defined by the distance between said third and fourth gate structures and a height of said third and fourth gate structures, and

said second gate aspect ratio is larger than a third gate aspect ratio that is defined by the distance between said fifth and sixth gate structures and a height of said fifth and sixth gate structures.

【Claim 8】 The semiconductor device according to claim 7, wherein said first and second gate aspect ratios are each larger than 0.8.

【Claim 9】 A semiconductor device manufacturing method, comprising the steps of:

(a) preparing a semiconductor substrate having a memory formation region where a memory device is to be formed and a logic formation region where a logic device

is to be formed;

(b) forming first and second impurity regions in an upper surface of said semiconductor substrate in said memory formation region and said logic formation region, respectively;

(c) forming first and second gate structures spaced apart at a given distance from each other on the upper surface of said semiconductor substrate in said memory formation region, and forming a third impurity region in an upper surface of said first impurity region between said first and second gate structures, said third impurity region having a conductivity type different from that of said first impurity region;

(d) forming third and fourth gate structures spaced apart at a given distance from each other on the upper surface of said semiconductor substrate in said logic formation region, and forming a fourth impurity region in an upper surface of said second impurity region between said third and fourth gate structures, said fourth impurity region having a different conductivity type from that of said second impurity region;

(e) applying a nondirectional sputtering method from above the structure obtained by said steps (c) and (d) to deposit a metal material on said third impurity region between said first and second gate structures and on said fourth impurity region between said third and fourth gate structures;

(f) causing said metal material and said semiconductor substrate to react with each other to form silicide films in the upper surfaces of said third and fourth impurity regions; and

(g) forming a capacitor above said silicide film in the upper surface of said third impurity region, said capacitor being electrically connected to said silicide film in the upper surface of said third impurity region;

a first gate aspect ratio that is defined by the distance between said first and

second gate structures and a height of said first and second gate structures being larger than a second gate aspect ratio that is defined by the distance between said third and fourth gate structures and a height of said third and fourth gate structures.

【Claim 10】 The semiconductor device manufacturing method according to claim 9, wherein said fourth impurity region is a source/drain region of a MOS transistor.

【Claim 11】 The semiconductor device manufacturing method according to either of claim 9 or 10, wherein said first gate aspect ratio is larger than 0.8.

【Claim 12】 The semiconductor device manufacturing method according to claim 9,

wherein in said step (b), a fifth impurity region is further formed in the upper surface of said semiconductor substrate in said logic formation region,

said semiconductor device manufacturing method further comprises the step (h) of, prior to said step (e), forming fifth and sixth gate structures spaced apart at a given distance from each other on the upper surface of said semiconductor substrate in said logic formation region and forming a sixth impurity region in an upper surface of said fifth impurity region between said fifth and sixth gate structures, said sixth impurity region having a conductivity type different from that of said fifth impurity region,

in said step (e), said nondirectional sputtering method is applied from above the structure obtained through said steps (c), (d), and (h) so as to deposit said metal material also on said sixth impurity region between said fifth and sixth gate structures,

in said step (f), said metal material and said semiconductor substrate are caused to react with each other to further form said silicide film also in the upper surface of said sixth impurity region, and

said second gate aspect ratio is larger than a third gate aspect ratio that is defined by the distance between said fifth and sixth gate structures and a height of said

fifth and sixth gate structures.

【Claim 13】 The semiconductor device manufacturing method according to claim 12, wherein each of said fourth and sixth impurity regions is a source/drain region of a MOS transistor.

【Claim 14】 The semiconductor device manufacturing method according to either of claim 12 or 13, wherein said first and second gate aspect ratios are each larger than 0.8.

【Detailed Description of the Invention】

【0001】

【Technical Field of the Invention】

The present invention relates to a memory/logic mixed semiconductor device in which memory and logic devices are fabricated on a semiconductor substrate, and to a method for manufacturing the same.

【0002】

【Prior Art】

In recent system LSIs, memory/logic mixed semiconductor devices are attracting attention in which large-capacity high-speed memory devices and logic devices are constructed on the same semiconductor substrate. Among them, as to semiconductor devices mounted with DRAMs suitable for large capacity applications, devices in which silicide films are formed within memory cells are developed to achieve higher speed memory devices.

【0003】

Patent document 1 discloses an example of such a memory/logic mixed semiconductor device having silicide films within memory cells. According to the technique described in the patent document 1, silicide films are formed on source/drain

regions and gate electrodes of transistors in both of a DRAM portion where DRAM resides and a logic portion where a logic device resides. Techniques about formation of silicide films are disclosed in patent documents 2-4.

【0004】

【Patent document 1】

Japanese Patent Application Laid-Open No. 2001-127270

【Patent document 2】

Japanese Patent Application Laid-Open No. 2000-269482

【Patent document 3】

Japanese Patent Application Laid-Open 8-31769 (1996)

【Patent document 4】

International Publication WO98/42009.

【0005】

【Problems to be Solved by the Invention】

In the memory/logic mixed semiconductor device described in the patent document 1, as shown in Fig. 6 of the patent document 1, the silicide film in the upper surfaces of source/drain regions in the DRAM portion and the silicide film in the upper surfaces of source/drain regions in the logic portion have the same thickness. Therefore, when the silicide film in the logic portion is formed thick to achieve higher speed of the logic device, then the silicide film in the DRAM portion, too, forms thick, which increases the leakage current of capacitors electrically connected to the source/drain regions. This deteriorates data storage characteristic of the DRAM. On the other hand, when the silicide film in the DRAM portion is formed thin to reduce the capacitor leakage current, then the silicide film in the logic portion also forms thin, which lowers operating speed of the logic device.

【0006】

Thus the present invention is produced in light of the above problems, and an object of the present invention is to provide a semiconductor technique that can achieve both of lowered resistance in a region where a logic device is formed and reduced leakage current of the capacitor of a memory device.

【0007】

【Means for Solving the Problems】

A semiconductor device according to the present invention comprises a semiconductor substrate having a memory formation region in which a memory device is formed and a logic formation region in which a logic device is formed, a first impurity region formed in an upper surface of said semiconductor substrate in said memory formation region, a second impurity region formed in the upper surface of said semiconductor substrate in said logic formation region, a third impurity region formed in an upper surface of said first impurity region and having a conductivity type different from that of said first impurity region, a fourth impurity region formed in an upper surface of said second impurity region and having a conductivity type different from that of said second impurity region, a first silicide film formed in an upper surface of said third impurity region, a capacitor formed above said first silicide film and electrically connected to said first silicide film, and a second silicide film formed in an upper surface of said fourth impurity region and having a larger thickness than said first silicide film.

【0008】

Further, a semiconductor device manufacturing method according to the present invention comprises the steps of (a) preparing a semiconductor substrate having a memory formation region where a memory device is to be formed and a logic formation region where a logic device is to be formed, (b) forming first and second impurity regions

in an upper surface of said semiconductor substrate in said memory formation region and said logic formation region, respectively, (c) forming first and second gate structures spaced apart at a given distance from each other on the upper surface of said semiconductor substrate in said memory formation region, and forming a third impurity region in an upper surface of said first impurity region between said first and second gate structures, said third impurity region having a conductivity type different from that of said first impurity region, (d) forming third and fourth gate structures spaced apart at a given distance from each other on the upper surface of said semiconductor substrate in said logic formation region, and forming a fourth impurity region in an upper surface of said second impurity region between said third and fourth gate structures, said fourth impurity region having a different conductivity type from that of said second impurity region, (e) applying a nondirectional sputtering method from above the structure obtained by said steps (c) and (d) to deposit a metal material on said third impurity region between said first and second gate structures and on said fourth impurity region between said third and fourth gate structures, (f) causing said metal material and said semiconductor substrate to react with each other to form silicide films in the upper surfaces of said third and fourth impurity regions, and (g) forming a capacitor above said silicide film in the upper surface of said third impurity region, said capacitor being electrically connected to said silicide film in the upper surface of said third impurity region, wherein a first gate aspect ratio that is defined by the distance between said first and second gate structures and a height of said first and second gate structures is larger than a second gate aspect ratio that is defined by the distance between said third and fourth gate structures and a height of said third and fourth gate structures.

【0009】

【Embodiments of the Invention】

First Embodiment

Fig. 1 is a cross-sectional view showing the structure of a semiconductor device according to a first embodiment of the invention. The semiconductor device of the first embodiment is a memory/logic mixed semiconductor device, where DRAM having CUB (Capacitor Under Bit Line) structure memory cells is adopted as the memory device and Dual-Gate salicide CMOS transistors are adopted as the logic device, for example.

【0010】

As shown in Fig. 1, the semiconductor device of the first embodiment has a semiconductor substrate 1 that is, for example, an n-type silicon substrate.. Element isolation insulating films 2 are formed in the upper surface of the semiconductor substrate 1 to divide the semiconductor substrate 1 into a plurality of regions.

【0011】

In a region where the memory device is formed (hereinafter referred to as a "memory formation region"), a p-type well region 3 is formed in the upper surface of the semiconductor substrate 1. In a region where the logic device is formed (hereinafter referred to as a "logic formation region"), a p-type well region 53 is formed in the upper surface of the semiconductor substrate 1.

【0012】

In the upper surface of the well region 3, a plurality of source/drain regions 4 are formed at given distances from each other, with cobalt silicide films 9 formed in their upper surfaces. In the upper surface of the well region 53, a plurality of source/drain regions 54 are formed at given distances from each other, with cobalt silicide films 59 formed in their upper surfaces. The source/drain regions 4 and 54 are both n-type impurity regions.

【0013】

In the memory formation region, a plurality of gate structures 5 are formed at given distances from each other on the semiconductor substrate 1. Each gate structure 5 is provided with a gate insulating film 6, a gate electrode 7 serving as a word line of DRAM memory cells, and sidewalls 8, with a cobalt silicide film 19 formed on top of the gate electrode 7. The gate insulating film 6, gate electrode 7 and cobalt silicide film 19 are stacked in this order on the semiconductor substrate 1, forming a stacked structure. The sidewalls 8 are formed on the sides of the stacked structure. Each gate structure 5 is positioned on the upper surface of the semiconductor substrate 1 between adjacent source/drain regions 4, with the cobalt silicide films 9 between adjacent gate structures 5.

【0014】

In the logic formation region, a plurality of gate structures 55 are formed at given distances on the semiconductor substrate 1. Each gate structure 55 is provided with a gate insulating film 56, a gate electrode 57, and sidewalls 58, with a cobalt silicide film 69 formed on top of the gate electrode 57. The gate insulating film 56, gate electrode 57 and cobalt silicide film 69 are stacked in this order above the semiconductor substrate 1, forming a stacked structure. The sidewalls 58 are formed on the sides of the stacked structure. Each gate structure 55 is positioned on the upper surface of the semiconductor substrate 1 between adjacent source/drain regions 54, with the cobalt silicide films 59 between adjacent gate structures 55.

【0015】

A gate structure 5, a pair of adjacent source/drain regions 4, and the well region 3 form an MOS transistor in a DRAM memory cell, and a gate structure 55, a pair of adjacent source/drain regions 54, and the well region 53 form an MOS transistor that functions as the logic device. The gate insulating films 6 and 56 are made of a film of silicon oxide and the gate electrodes 7 and 57 are made of a film of polycrystalline silicon,

for example.

【0016】

The cobalt silicide films 9 in the memory formation region are thinner than the cobalt silicide films 59 in the logic formation region. Thus the film thickness tm of the cobalt silicide films 9 is smaller than the film thickness tr1 of the cobalt silicide films 59.

【0017】

The gate structures 5 and 55 have the same height, h, and the distance dm between adjacent gate structures 5 is smaller than the distance dr1 between adjacent gate structures 55. Therefore the gate aspect ratio in the memory formation region is larger than the gate aspect ratio in the logic formation region.

【0018】

Now, the gate aspect ratio is the ratio between the gate structure height and the distance between adjacent gate structures. More specifically, the gate aspect ratio in the memory formation region is obtained by dividing the height h of the gate structure 5 by the distance dm between adjacent gate structures 5. The gate aspect ratio in the logic formation region is obtained by dividing the height h of the gate structure 55 by the distance dr1 between adjacent gate structures 55. Hereinafter, the value obtained by dividing the height h of the gate structure 5 by the distance dm between gate structures 5 is referred to as a "first gate aspect ratio" and the value obtained by dividing the height h of the gate structure 55 by the distance dr1 between gate structures 55 is referred to as a "second gate aspect ratio."

【0019】

In the first embodiment, the first gate aspect ratio is set larger than 0.8 and the second gate aspect ratio is set equal to or less than 0.8.

【0020】

An interlayer insulating film 20 is formed over the semiconductor substrate 1 in the memory formation region and logic formation region, covering the gate structures 5 and 55 and cobalt silicide films 19 and 69. A plurality of contact plugs 10 are formed in the interlayer insulating film 20 and connected to the cobalt silicide films 9. The source/drain regions 4 and the contact plugs 10 are thus electrically connected to each other. The upper surfaces of the contact plugs 10 are exposed from the interlayer insulating film 20.

【0021】

An insulating layer 23, including interlayer insulating films 21 and 22, is formed over the interlayer insulating film 20 and contact plugs 10. A plurality of DRAM memory cell capacitors 11 are formed in the insulating layer 23; each capacitor 11 has a lower electrode 12, a dielectric film 13, and an upper electrode 14. Each upper electrode 14 is positioned opposite to the lower electrode 12 with the dielectric film 13 between them.

【0022】

The lower electrodes 12 of capacitors 11 are connected to some of the plurality of contact plugs 10, specifically to contact plugs 10 that are each electrically connected to one of adjacent source/drain regions 4. The cobalt silicide film 9 formed in one of adjacent source/drain regions 4 and the capacitor 11 are thus electrically connected to each other.

【0023】

A plurality of contact plugs 15 are formed in the insulating layer 23. The contact plugs 15 are connected to contact plugs 10 that are not electrically connected to capacitors 11. Also, a plurality of contact plugs 60 are formed in the interlayer insulating film 20 and insulating layer 23. The contact plugs 60 are connected to the

cobalt silicide films 59 in the source/drain regions 54. The top surfaces of the contact plugs 15 and 60 are exposed from the insulating layer 23.

【0024】

On the insulating layer 23, metal interconnection 16 lies in contact with the contact plugs 15 and metal interconnection 66 lies in contact with the contact plugs 60. The metal interconnection 16 is a DRAM memory cell bit line which is located above the capacitors 11.

【0025】

In this way, in the semiconductor device of the first embodiment, the cobalt silicide films 9 in the upper surfaces of the source/drain regions 4 are thinner than the cobalt silicide films 59 in the upper surfaces of the source/drain regions 54. Therefore the distances between the cobalt silicide films 9 and the well region 3 are longer than the distances between the cobalt silicide films 59 and the well region 53. Therefore the leakage current between the source/drain regions 4 and the well region 3 can be reduced to be lower than the leakage current between the source/drain regions 54 and the well region 53.

【0026】

On the other hand, since the cobalt silicide films 59 are thicker than the cobalt silicide films 9, the source/drain regions 54 exhibit a lower resistance than the source/drain regions 4. It is thus possible to achieve both of a reduction in resistance of the source/drain regions 54 in the logic formation region and a reduction in leakage current of the capacitors 11 electrically connected to the cobalt silicide films 9.

【0027】

Furthermore, the presence of cobalt silicide films 59 in the source/drain regions 54 enables high speed operation of MOS transistors in the logic formation region.

【0028】

Next, a method for manufacturing the semiconductor device of Fig. 1 is described. Figs. 2 to 7 are cross-sectional views showing a sequence of process steps for manufacturing the semiconductor device of Fig. 1. First, as shown in Fig. 2, element isolation insulating films 2 are formed in the upper surface of the semiconductor substrate 1 by a known LOCOS isolation technique or trench isolation technique. Then, well regions 3 and 53 are formed in the upper surface of the semiconductor device 1 in the memory formation region and logic formation region, respectively.

【0029】

Next, by thermally oxidizing the semiconductor substrate 1, for example, a silicon oxide film is formed on the upper surface of the semiconductor substrate 1, and then a polycrystalline silicon film is formed all over the surface. Then, the silicon oxide film and polycrystalline silicon film are etched using a resist having a given opening pattern. Thus, as shown in Fig. 3, the gate insulating films 6 and gate electrodes 7 are formed in the memory formation region and the gate insulating films 56 and gate electrodes 57 are formed in the logic formation region.

【0030】

Next, using the element isolation insulating films 2, gate insulating films 6, 56, and gate electrodes 7, 57 as masks, an impurity, e.g. phosphorus or arsenic, is ion-implanted at a relatively low concentration into the upper surface of the semiconductor substrate 1. Thus, as shown in Fig. 3, n^--type impurity regions 4a are formed in the upper surface of the semiconductor substrate 1 in the memory formation region, and n^--type impurity regions 54a are formed in the upper surface of the semiconductor substrate 1 in the logic formation region.

【0031】

Next, a silicon nitride film is formed by, e.g. CVD, all over the surface, and then etched by an anisotropic dry etching process presenting a high etch rate in the depth direction of the semiconductor substrate 1. This forms, as shown in Fig. 4, sidewalls 8 and 58, both of which are of silicon nitride film, whereby the gate structures 5 and 55 are completed on the semiconductor substrate 1.

【0032】

Next, using the gate structures 5 and 55 and the element isolation insulating films 2 as masks, an impurity, e.g. phosphorus or arsenic, is ion-implanted into the upper surface of the semiconductor substrate 1 at a relatively high concentration. Thus, as shown in Fig. 4, n^+-type impurity regions 4b are formed in the upper surface of the semiconductor substrate 1 in the memory formation region, and n^+-type impurity regions 54b are formed in the upper surface of the semiconductor substrate 1 in the logic formation region.

【0033】

Through the process steps described referring to Figs. 3 and 4, a plurality of gate structures 5 are formed on the semiconductor substrate 1 in the memory formation region, and source/drain regions 4, including impurity regions 4a and 4b, are formed in the upper surface of the well region 3 between adjacent gate structures 5, whereby MOS transistors in DRAM memory cells are completed. Also, in the logic formation region, a plurality of gate structures 55 are formed on the semiconductor substrate 1 and source/drain regions 54 including impurity regions 54a, 54b are formed in the upper surface of the well region 53 between adjacent gate structures 55, whereby MOS transistors serving as the logic device are completed.

【0034】

Next, as shown in Fig. 5, a metal material 25 of cobalt is deposited all over the

surface from above the structure shown in Fig. 4 by using a nondirectional sputtering method. Now, unlike a sputtering method with good linearity, such as collimation sputtering method, the nondirectional sputtering method uses no special means to restrict directions of metal material sputtered off the target to the depth direction of the semiconductor substrate. Therefore, the nondirectional sputtering method allows metal material sputtered off the target to be deposited on the semiconductor substrate with vectors in all directions.

【0035】

When metal material is thus deposited by such a nondirectional sputtering method from above the semiconductor substrate having a plurality of gate structures at given intervals, then the film thickness of metal material deposited on the source/drain regions between adjacent gate structures depends on the gate aspect ratio. As previously stated, the nondirectional sputtering method allows the metal material to scatter with vectors in all directions. Accordingly, with a larger aspect ratio, a thicker film of metal material is deposited on sides of the gate structures, while a thinner film of metal material is deposited on the source/drain regions.

【0036】

In the first embodiment, the first gate aspect ratio defined by the height of the gate structures 5 in the memory formation region and the distance between gate structures 5 is set larger than the second gate aspect ratio defined by the height of the gate structures 55 in the logic formation region and the distance between gate structures 55. Therefore, when metal material 25 is deposited all over the surface by using the nondirectional sputtering method, as shown in Fig. 5, the thickness tmm of the metal material 25 on the source/drain regions 4 is smaller than the thickness tmr1 of the metal material 25 on the source/drain regions 54.

【0037】

Next, a thermal process with a lamp annealing apparatus, for example, is performed to cause the metal material 25 and the silicon in contact with it to react with each other. That is, a reaction is caused between the metal material 25 and the semiconductor substrate 1 and gate electrodes 7 and 57 that are in contact with it. Then unreacted portion of the metal material 25 is removed.

【0038】

Thus, as shown in Fig. 6, the upper surface of the semiconductor substrate 1 is partially silicidized to form cobalt silicide films 9 and 59 in the upper surfaces of the source/drain regions 4 and 54, respectively. At the same time, the top surfaces of the gate electrodes 7 and 57 are silicidized to form cobalt silicide films 19 and 69 on the gate electrodes 7 and 57, respectively.

【0039】

During this process, because the film thickness tmm of the metal material 25 deposited on the source/drain regions 4 is smaller than the film thickness tmr1 of the metal material 25 deposited on the source/drain regions 54, the film thickness tm of the cobalt silicide films 9 in the source/drain regions 4 is smaller than the film thickness tr1 of the cobalt silicide films 59 in the source/drain regions 54.

【0040】

Next, as shown in Fig. 7, the interlayer insulating film 20 is formed over the semiconductor substrate 1 to cover the gate structures 5, 55 and cobalt silicide films 19, 69. Then contact plugs 10 are formed in the interlayer insulating film 20. Specifically, first, a resist having a given opening pattern (not shown) is formed on the interlayer insulating film 20. Next, the interlayer insulating film 20 is etched using this resist to form, in the interlayer insulating film 20, contact holes (not shown) that reach the cobalt

silicide films 9. Then contact plugs are formed to fill the contact holes, whereby a plurality of contact plugs 10 are formed in the interlayer insulating film 20.

【0041】

Next, interlayer insulating film 21 is formed on the interlayer insulating film 20 and contact plugs 10. Then openings (not shown) are formed in the interlayer insulating film 21 to expose the contact plugs 10 that are each electrically connected to one of adjacent source/drain regions 4.

【0042】

Next, as shown in Fig. 7, DRAM memory cell capacitors 11 are formed in the openings, so that they are in contact with the exposed contact plugs 10. Specifically, first, a metal film containing a refractory metal, e.g. ruthenium, is formed all over the surface. Then, with the openings covered with resist, the metal film on the upper surface of the interlayer insulating film 21 is removed by anisotropic dry etching. Thus lower electrodes 12 of capacitors 11 that contain refractory metal, e.g. ruthenium, are formed in the openings. Next, an insulating film of, e.g. ditantalum pentoxide, and a metal film that contains a refractory metal, e.g. ruthenium, are stacked in this order all over the surface, which are then patterned using resist. Thus the dielectric films 13 of capacitors 11, that are made of ditantalum pentoxide, and the upper electrodes 14 of capacitors 11, that contain refractory metal, e.g. ruthenium, are formed, whereby the capacitors 11 are completed in the openings.

【0043】

Next, interlayer insulating film 22 is formed all over the surface and planarized by CMP method. The interlayer insulating film 22 covering the capacitors 11 is thus formed on the interlayer insulating film 21, whereby the insulating layer 23 is completed.

【0044】

Next, contact holes (not shown) are formed through the insulating layer 23 to expose contact plugs 10 that are not electrically connected with capacitors 11, and contact holes (not shown) are formed through the insulating layer 23 and interlayer insulating film 20 to expose the cobalt silicide films 59 in the logic formation region. Then the contact holes are filled with contact plugs, so as to form contact plugs 15 through the insulating layer 23 and contact plugs 60 through the insulating layer 23 and interlayer insulating film 20.

【0045】

Next, metal interconnection 16 in contact with the contact plugs 15 and metal interconnection 66 in contact with the contact plugs 60 are formed on the insulating layer 23.

【0046】

The semiconductor device of Fig. 1 of the first embodiment is thus completed through the process steps shown above.

【0047】

In this way, in the first embodiment, the first gate aspect ratio in the memory formation region is larger than the second gate aspect ratio in the logic formation region, so that the nondirectional sputtering method causes the metal material 25 to be deposited thinner on the source/drain regions 4 than on the source/drain regions 54. Therefore the cobalt silicide films 9 in the upper surfaces of the source/drain regions 4 are thinner than the cobalt silicide films 59 in the upper surfaces of the source/drain regions 54.

【0048】

In other words, the cobalt silicide films 9 can be easily formed thinner than the cobalt silicide films 59 through the nondirectional sputtering method since the first gate aspect ratio is larger than the second gate aspect ratio.

【0049】

Therefore the leakage current between the source/drain regions 4 and the well region 3 is lower than the leakage current between the source/drain regions 54 and the well region 53.

【0050】

On the other hand, since the cobalt silicide films 59 are thicker than the cobalt silicide films 9, the resistance of the source/drain regions 54 is lower than that of the source/drain regions 4. It is thus possible to achieve both of lowered resistance of the source/drain regions 54 in the logic formation region and reduced leakage current of capacitors 11 electrically connected to the cobalt silicide films 9.

【0051】

Furthermore, since the first gate aspect ratio is larger than 0.8 in the first embodiment, it is easy to form thinner cobalt silicide films 9 in the memory formation region. This is now described.

【0052】

Fig. 8 is a diagram showing the relation between the gate aspect ratio and silicide film thickness. In Fig. 8, the solid line shows a characteristic obtained when the nondirectional sputtering method is used to form silicide film and the one-dot-chain line shows a characteristic obtained when the sputtering method with good linearity is used. As shown in Fig. 8, when the gate aspect ratio exceeds 0.8, the silicide film thickness rapidly decreases at an increasing rate of variation. Therefore, the cobalt silicide films 9 can easily be formed thin by setting the first gate aspect ratio larger than 0.8 as explained in the first embodiment.

【0053】

Second Embodiment

Fig. 9 is a cross-sectional view showing the structure of a semiconductor device according to a second embodiment of the invention. According to the second embodiment, basically, the semiconductor device as shown in the first embodiment further includes, in the logic formation region, a region having a gate aspect ratio that is larger than the second gate aspect ratio. In the second embodiment, the region having the second gate aspect ratio described in the first embodiment is referred to as a "first region" and the region having a gate aspect ratio larger than the second gate aspect ratio, an additional region introduced in the second embodiment, is referred to as a "second region."

【0054】

As shown in Fig. 9, the semiconductor device of the second embodiment has a p-type well region 83 that is formed in the second region of the logic formation region in the upper surface of the semiconductor substrate 1. In the upper surface of the well region 83, a plurality of source/drain regions 84 are formed at given distances from each other and cobalt silicide films 89 are formed in their upper surfaces. The source/drain regions 84 are n-type impurity regions.

【0055】

In the second region, a plurality of gate structures 85 are formed at given distances on the semiconductor substrate 1. Each gate structure 85 is provided with a gate insulating film 86, a gate electrode 87, and sidewalls 88, with a cobalt silicide film 99 formed on top of the gate electrode 87. The gate insulating film 86, gate electrode 87 and cobalt silicide film 99 are stacked in this order on the semiconductor substrate 1, forming a stacked structure. The sidewalls 88 are formed on sides of the stacked structure. Each gate structure 85 is located on the upper surface of the semiconductor substrate 1 between adjacent source/drain regions 84, with the cobalt silicide films 89

between adjacent gate structures 85.

【0056】

A gate structure 85, a pair of adjacent source/drain regions 84, and the well region 83 form an MOS transistor serving as the logic device. The gate insulating films 86 are made of silicon oxide film and the gate electrodes 87 are made of polycrystalline silicon film, for example.

【0057】

The cobalt silicide films 89 in the second region are thicker than the cobalt silicide films 9 in the memory formation region and the cobalt silicide films 59 in the first region. Thus the film thickness tm of the cobalt silicide films 9 is smaller than the film thickness tr1 of the cobalt silicide films 59, which is smaller than the film thickness tr2 of the cobalt silicide films 89.

【0058】

The height h of the gate structures 85 is equal to that of the gate structures 5, 55, and the distance dr2 between adjacent gate structures 85 is larger than the distance dm between gate structures 5 and the distance dr1 between gate structures 55. Therefore the gate aspect ratio in the second region, which is obtained by dividing the height h of the gate structures 85 by the distance dr2 between gate structures 85, is larger than the first gate aspect ratio in the memory formation region and the second gate aspect ratio in the first region. The gate aspect ratio in the second region is hereinafter referred to as a "third gate aspect ratio."

【0059】

While the second gate aspect ratio of the first embodiment is set equal to or less than 0.8, the first and second gate aspect ratios of the second embodiment are set larger than 0.8 and the third gate aspect ratio is set equal to or less than 0.8.

【0060】

The interlayer insulating film 20 on the semiconductor substrate 1 extends also in the second region, covering the gate structures 85 and cobalt silicide films 99. The insulating layer 23 on the interlayer insulating film 20 also extends in the second region.

【0061】

In the second region, a plurality of contact plugs 90 are formed in the insulating layer 23 and interlayer insulating film 20. The contact plugs 90 are connected to the cobalt silicide films 89 in the source/drain regions 84, with the upper surfaces thereof exposed from the insulating layer 23. Then on the insulating layer 23 in the second region, metal interconnection 96 lies in contact with the contact plugs 90.

【0062】

Thus, in the semiconductor device of the second embodiment, the cobalt silicide films 89 are thicker than the cobalt silicide films 59, so that the resistance of the source/drain regions 84 is lower than that of the source/drain regions 54. Therefore, by using the source/drain regions 54 to form an electrical circuit whose operating speed is crucial, e.g. a circuit called "critical path" that determines speed performance of the logic device, it is possible to certainly allow that circuit to operate at an enhanced speed, resulting in an enhanced operating speed of the entire logic device.

【0063】

On the other hand, since the cobalt silicide films 59 are thinner than the cobalt silicide films 89, the leakage current between the source/drain regions 54 and the well region 53 is lower than the leakage current between the source/drain regions 84 and the well region 83. Therefore, a circuit in the logic device other than the critical path, i.e. a circuit whose operating speed is not crucial, can be formed in the first region, and then it is possible to ensure high speed operation of the circuit where operating speed is crucial,

while suppressing an increase in leakage current of the entire logic device.

【0064】

Furthermore, the presence of the cobalt silicide films 59 in the source/drain regions 54 and the presence of the cobalt silicide films 59 in the source/drain regions 84 enable high speed operation of the MOS transistors fabricated in the logic formation region.

【0065】

Next, a method for manufacturing the semiconductor device of Fig. 9 is described. Figs. 10 to 15 are cross-sectional views showing a sequence of process steps for manufacturing the semiconductor device of Fig. 9. First, as shown in Fig. 10, element isolation insulating films 2 are formed in the upper surface of the semiconductor substrate 1 and then well regions 3 and 53, and the well region 83 in the second region of the logic formation region, are formed in the upper surface of the semiconductor substrate 1.

【0066】

Next, by thermally oxidizing the semiconductor substrate 1, for example, a silicon oxide film is formed on the upper surface of the semiconductor substrate 1 and then a polycrystalline silicon film is formed all over the surface. Then, the silicon oxide film and polycrystalline silicon film are etched using a resist having a given opening pattern. As shown in Fig. 11, this forms the gate insulating films 6, 56 and gate electrodes 7, 57, and the gate insulating films 86 and gate electrodes 87 in the second region.

【0067】

Next, using as masks the element isolation insulating films 2, gate insulating films 6, 56, 86 and gate electrodes 7, 57, 87, an impurity, e.g. phosphorus or arsenic, is

ion-implanted at a relatively low concentration into the upper surface of the semiconductor substrate 1. As shown in Fig. 11, this forms the impurity regions 4a and 54a, and also forms n^--type impurity regions 84a in the upper surface of the semiconductor substrate 1 in the second region.

【0068】

Next, a silicon nitride film is formed all over the surface by, e.g. CVD method, and then etched by an anisotropic dry etching process presenting a high etch rate in the depth direction of the semiconductor substrate 1. Thus, as shown in Fig. 12, sidewalls 8 and 58, and sidewalls 88 of silicon nitride film, are formed, whereby the gate structures 5, 55, 85 are completed on the semiconductor substrate 1.

【0069】

Next, using the gate structures 5, 55, 85 and the element isolation insulating films 2 as masks, an impurity, e.g. phosphorus or arsenic, is ion-implanted into the upper surface of the semiconductor substrate 1 at a relatively high concentration. Then, as shown in Fig. 12, the impurity regions 4b, 54b, and n^+-type impurity regions 84b in the second region, are formed in the upper surface of the semiconductor substrate 1.

【0070】

Through the process steps described referring to Figs. 11 and 12, a plurality of gate structures 85 are formed in the second region of the semiconductor substrate 1, and source/drain regions 84, including impurity regions 84a, 84b, are formed in the upper surface of the well region 83 between adjacent gate structures 85, whereby MOS transistors serving as the logic device are completed.

【0071】

Next, as shown in Fig. 13, the nondirectional sputtering method is applied from above the structure of Fig. 12 to deposit metal material 25 of cobalt all over the surface.

As previously described, when metal material 25 is deposited by the nondirectional sputtering method, a larger gate aspect ratio causes the metal material to be deposited to a smaller film thickness on the source/drain regions. In the second embodiment, the first gate aspect ratio is larger than the second gate aspect ratio, which is larger than the third gate aspect ratio. Therefore, as shown in Fig. 13, the thickness tmm of the metal material 25 on the source/drain regions 4 is smaller than the thickness tmr1 of the metal material 25 on the source/drain regions 54, which is smaller than the thickness tmr2 of the metal material 25 on the source/drain regions 84.

【0072】

Next, a thermal process with a lamp annealing apparatus, for example, is performed to cause the metal material 25 and the silicon in contact with it to react with each other. That is, a reaction is caused between the metal material 25 and the semiconductor substrate 1 and gate electrodes 7, 57, 87 that are in contact with it. Then unreacted portion of metal material 25 is removed.

【0073】

Thus, as shown in Fig. 14, the upper surface of the semiconductor substrate 1 is partially silicidized to form cobalt silicide films 9 and 59, and to form cobalt silicide films 89 in the upper surfaces of the source/drain regions 84. At the same time, the top surfaces of the gate electrodes 7, 57, 87 are silicidized to form cobalt silicide films 19 and 69, and cobalt silicide films 99 on the gate electrodes 87.

【0074】

At this point, since the film thickness tmm of the metal material 25 deposited on the source/drain regions 4 is smaller than the film thickness tmr1 of the metal material 25 deposited on the source/drain regions 54, which is smaller than the film thickness tmr2 of the metal material 25 deposited on the source/drain regions 84, the film thickness tm of

the cobalt silicide films 9 on the source/drain regions 4 is smaller than the film thickness tr1 of the cobalt silicide films 59 on the source/drain regions 54, which is smaller than the film thickness tr2 of the cobalt silicide films 89 on the source/drain regions 84.

【0075】

Next, as shown in Fig. 15, the interlayer insulating film 20 is formed all over the surface to cover the gate structures 5, 55, 85 and cobalt silicide films 19, 69, 99. Then contact plugs 10 are formed in the manner described previously.

【0076】

Next, the interlayer insulating film 21 is formed over the interlayer insulating film 20 and contact plugs 10, and DRAM memory cell capacitors 11 are formed in the interlayer insulating film 21 in the above-described manner.

【0077】

Next, interlayer insulating film 22 is formed all over the surface and planarized by CMP method. The interlayer insulating film 22 covering the capacitors 11 is thus formed on the interlayer insulating film 21, whereby the insulating layer 23 is completed.

【0078】

Next, contact holes (not shown) are formed in the insulating layer 23 to expose contact plugs 10 that are not electrically connected with capacitors 11, and contact holes (not shown) for exposing cobalt silicide films 59 in the first region, and contact holes (not shown) for exposing cobalt silicide films 89 in the second region, are formed in the insulating layer 23 and interlayer insulating film 20. Then the contact holes are filled with contact plugs, completing contact plugs 15, 60, and contact plugs 90 in the second region in the insulating layer 23 and interlayer insulating film 20.

【0079】

Next, metal interconnections 16 and 66, and metal interconnection 96 in contact

with the contact plugs 90, are formed on the insulating layer 23.

【0080】

The semiconductor device of Fig. 9 of the second embodiment is thus completed through the process steps shown above.

【0081】

In this way, in the second embodiment, the third gate aspect ratio in the second region is smaller than the second gate aspect ratio in the first region, so that the cobalt silicide films 89 in the second region form thicker than the cobalt silicide films 59 in the first region.

【0082】

In other words, the cobalt silicide films 89 can be easily formed thicker than the cobalt silicide films 59 through the nondirectional sputtering method because the second gate aspect ratio is larger than the third gate aspect ratio.

【0083】

Thus the resistance of the source/drain regions 84 is lower than that of the source/drain regions 54. Therefore, the circuit whose operating speed is crucial can be fabricated using the source/drain regions 84 so as to ensure its enhanced operating speed.

【0084】

On the other hand, since the cobalt silicide films 59 are thinner than the cobalt silicide films 89, the leakage current between the source/drain regions 54 and well region 53 is lower than the leakage current between the source/drain regions 84 and well region 83. Therefore, the circuit whose operating speed is not crucial can be fabricated in the first region, and then it is possible to ensure high speed operation of the circuit where operating speed is crucial, while suppressing the leakage current of the entire logic device.

【0085】

Furthermore, in the second embodiment, since the first and second gate aspect ratios are both set larger than 0.8, the cobalt silicide films 9 in the memory formation region and the cobalt silicide films 59 in the first region can both be formed thinner easily for the reason described earlier.

【0086】

【Advantageous Effect of the Invention】

In a semiconductor device according to the present invention, the first silicide film in the memory formation region is thinner than the second silicide film in the logic formation region, so that the leakage current between the first and third impurity regions is lower than the leakage current between the second and fourth impurity regions. On the other hand, since the second silicide film is thicker than the first silicide film, the resistance of the fourth impurity region is lower than that of the third impurity region. Thus it is possible to achieve both of lowered resistance of the fourth impurity region in the logic formation region and reduced leakage current of the capacitor electrically connected to the first silicide film.

【0087】

Further, according to a semiconductor device manufacturing method of the present Invention, since the first gate aspect ratio is larger than the second gate aspect ratio, the use of the nondirectional sputtering method in step (e) causes the metal material to form thinner on the third impurity region than on the fourth impurity region. This causes in step (f) the silicide film to form thinner in the upper surface of the third impurity region than in the upper surface of the fourth impurity region. This makes the leakage current between the first and third impurity regions lower than the leakage current between the second and fourth impurity regions. On the other hand, since the silicide

film in the upper surface of the fourth impurity region is thicker than the silicide film in the upper surface of the third impurity region, the fourth impurity region presents a lower resistance than the third impurity region. Thus it is possible to achieve both of lowered resistance of the fourth impurity region in the logic formation region and reduced leakage current of the capacitor electrically connected to the first silicide film.

【Brief Description of the Drawings】

【Fig. 1】 is a cross-sectional view showing the structure of a semiconductor device according to a first embodiment of the invention;

【Fig. 2】 is a cross-sectional view showing a sequence of process steps for manufacturing the semiconductor device of the first embodiment of the invention;

【Fig. 3】 is a cross-sectional view showing a sequence of process steps for manufacturing the semiconductor device of the first embodiment of the invention;

【Fig. 4】 is a cross-sectional view showing a sequence of process steps for manufacturing the semiconductor device of the first embodiment of the invention;

【Fig. 5】 is a cross-sectional view showing a sequence of process steps for manufacturing the semiconductor device of the first embodiment of the invention;

【Fig. 6】 is a cross-sectional view showing a sequence of process steps for manufacturing the semiconductor device of the first embodiment of the invention;

【Fig. 7】 is a cross-sectional view showing a sequence of process steps for manufacturing the semiconductor device of the first embodiment of the invention;

【Fig. 8】 is a diagram showing a relation between gate aspect ratio and silicide film thickness;

【Fig. 9】 is a cross-sectional view showing the structure of a semiconductor device according to a second embodiment of the invention; and

【Fig. 10】 is a cross-sectional view showing a sequence of process steps for

manufacturing the semiconductor device of the second embodiment of the invention.

【Fig. 11】 is a cross-sectional view showing a sequence of process steps for manufacturing the semiconductor device of the second embodiment of the invention.

【Fig. 12】 is a cross-sectional view showing a sequence of process steps for manufacturing the semiconductor device of the second embodiment of the invention.

【Fig. 13】 is a cross-sectional view showing a sequence of process steps for manufacturing the semiconductor device of the second embodiment of the invention.

【Fig. 14】 is a cross-sectional view showing a sequence of process steps for manufacturing the semiconductor device of the second embodiment of the invention.

【Fig. 15】 is a cross-sectional view showing a sequence of process steps for manufacturing the semiconductor device of the second embodiment of the invention.

【Explanation of Referenced Numerals】

1 semiconductor substrate; 3, 53, 83 well region; 4, 54, 84 source/drain region; 5, 55, 85 gate structure; 9, 59, 89 cobalt silicide film; 11 capacitor; 25 metal material

【Document Name】 Abstract

【Abstract】

【Problems to be Solved】

A semiconductor technique is provided which can achieve both of lowered resistance in a logic formation region and reduced leakage current of the capacitor of a memory device.

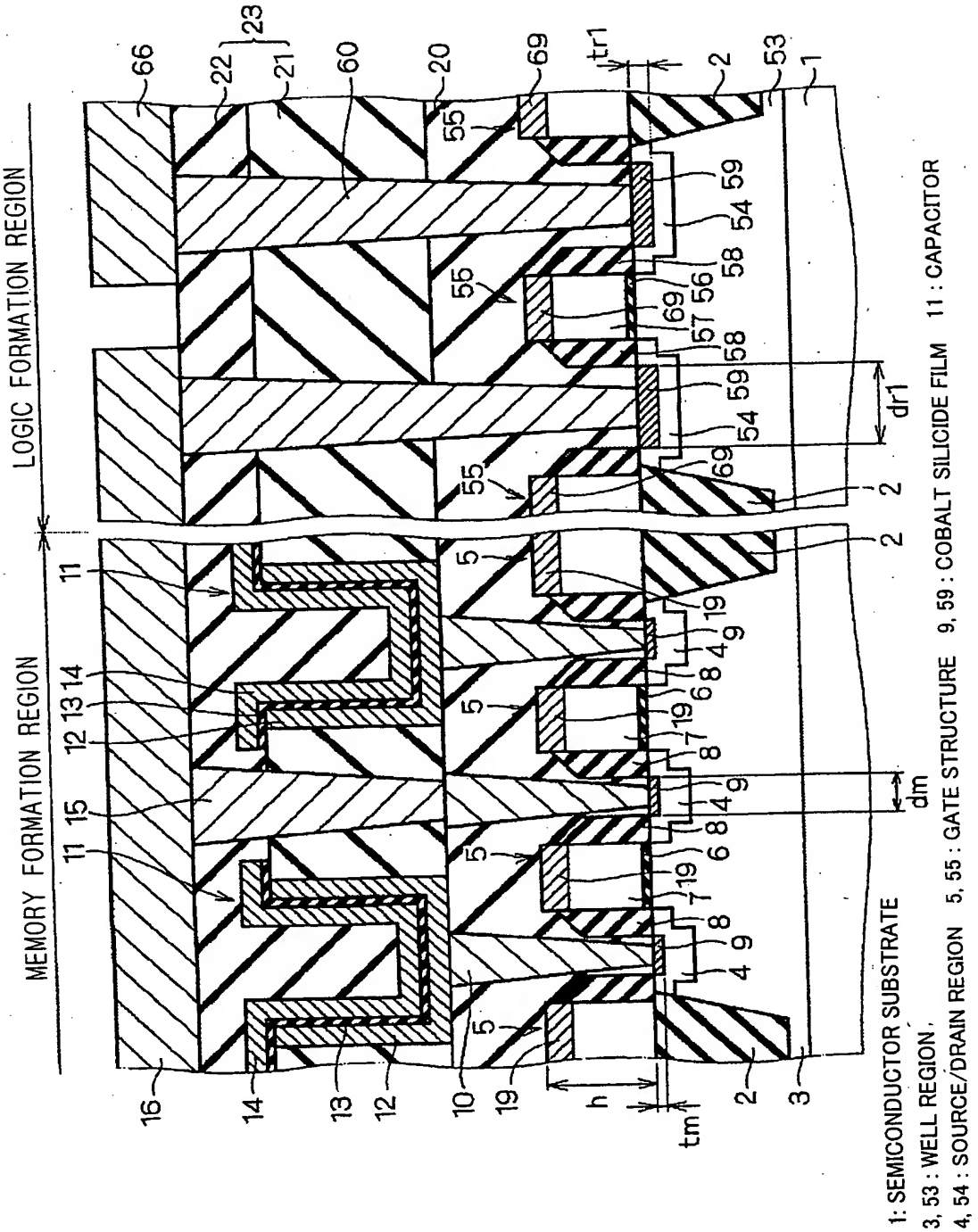
【Means to Solve the Problems】

Source/drain regions 4 are formed in the upper surface of a semiconductor substrate 1 in a memory formation region and cobalt silicide films 9 are formed in the upper surfaces of the source/drain regions 4. Source/drain regions 54 are formed in the upper surface of the semiconductor substrate 1 in a logic formation region and cobalt silicide films 59 are formed in the upper surfaces of the source/drain regions 54. The cobalt silicide films 59 in the logic formation region are thicker than the cobalt silicide films 9 in the memory formation region.

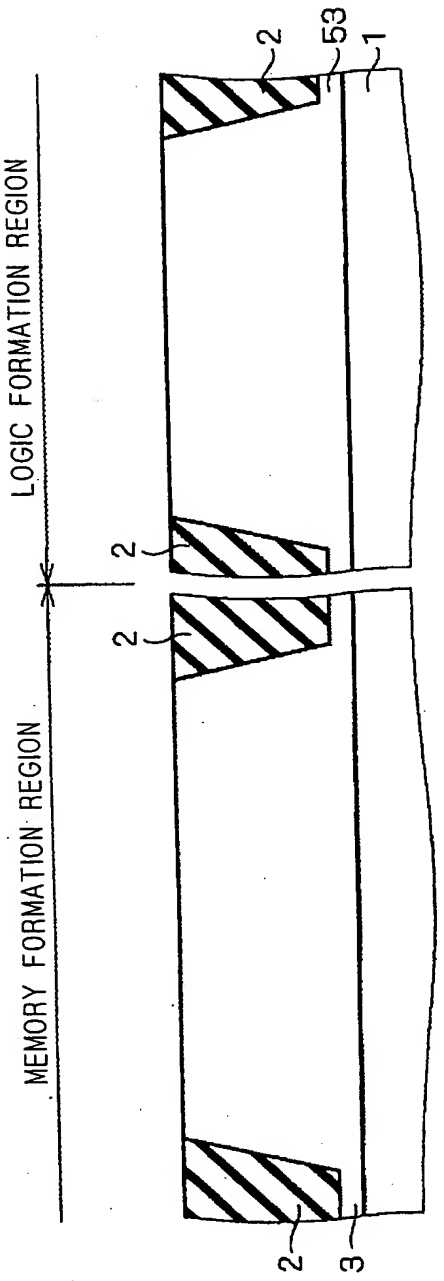
【Selected Figure】 Fig. 1

【Document Name】 Drawings

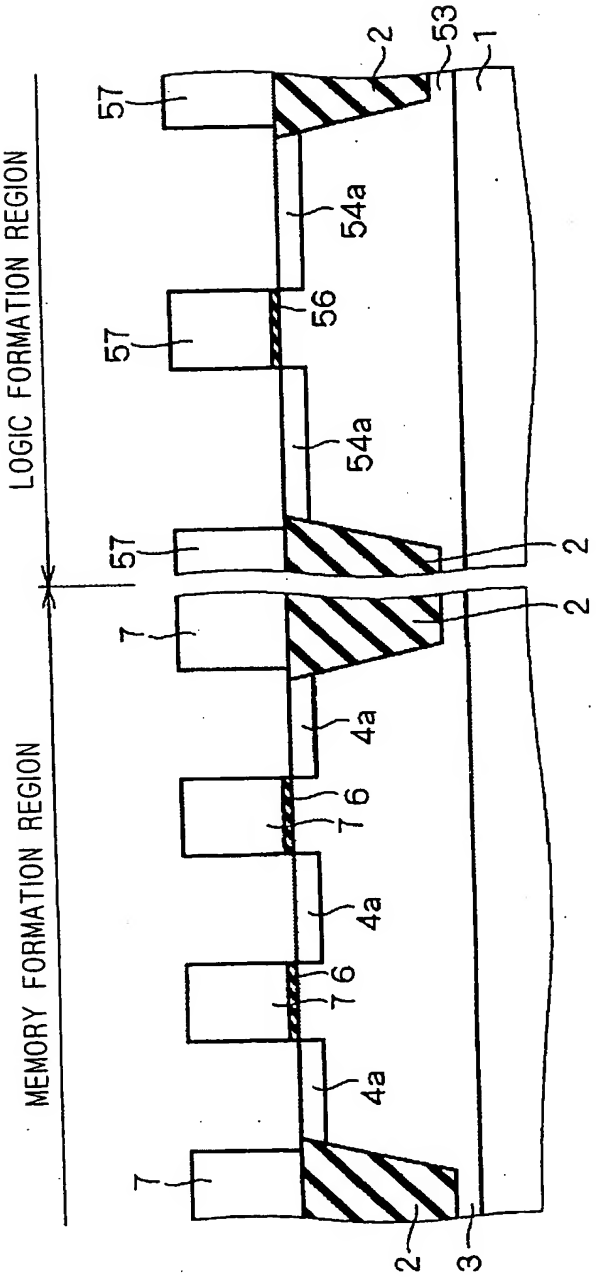
【Fig. 1】



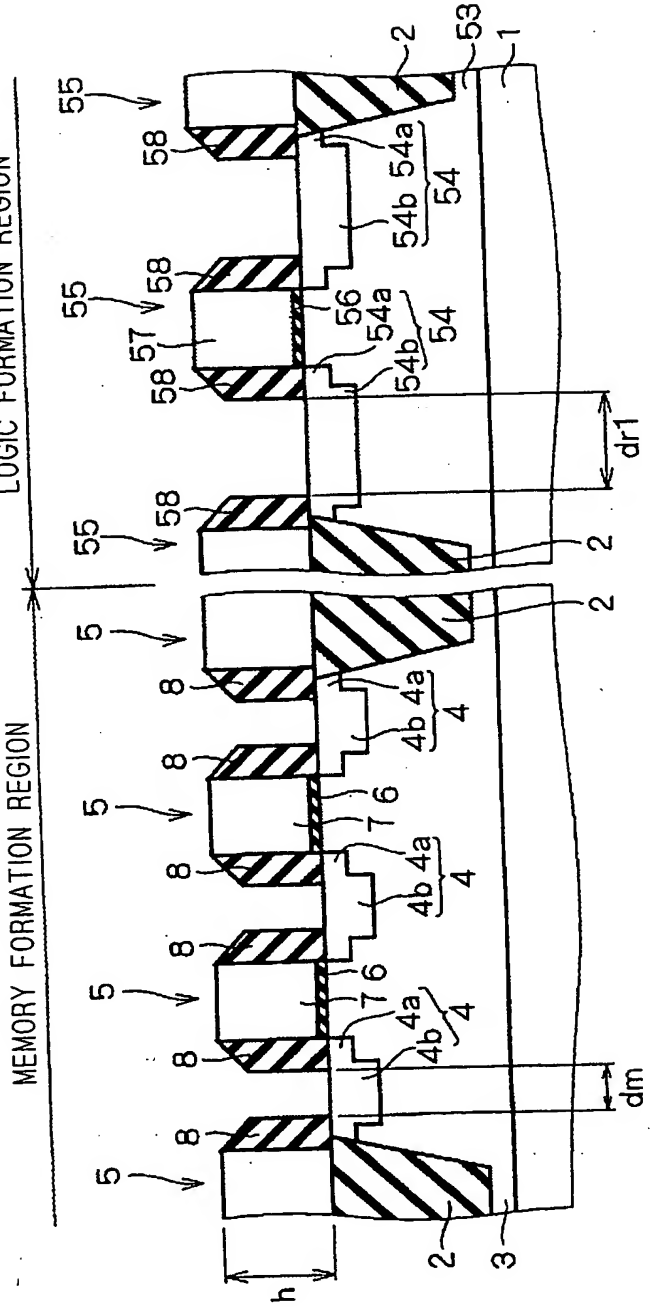
【Fig. 2】



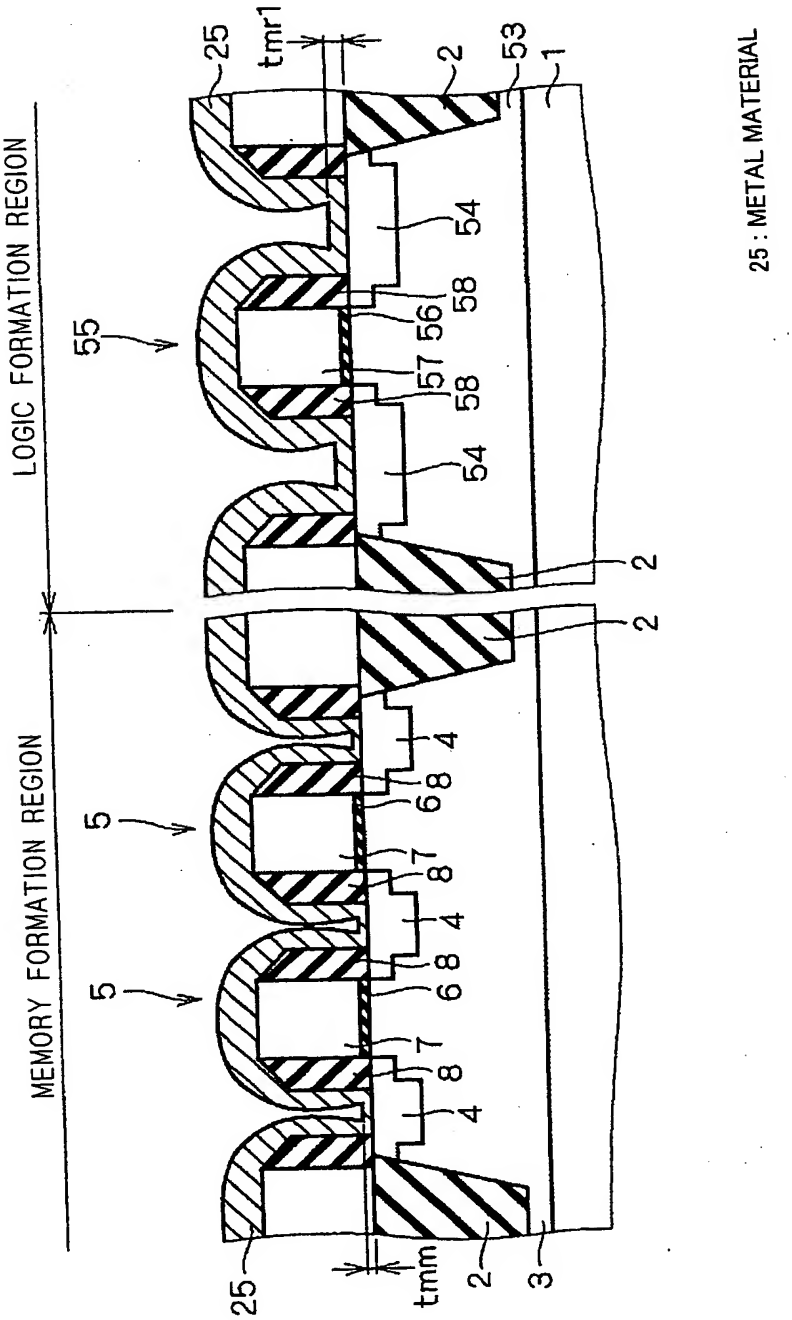
【Fig. 3】


LOGIC FORMATION REGION
MEMORY FORMATION REGION
57
57
57
7
7
2
53
1
54a
54a
56
2
2
4a
4a
4a
6
6
7
7
2
3

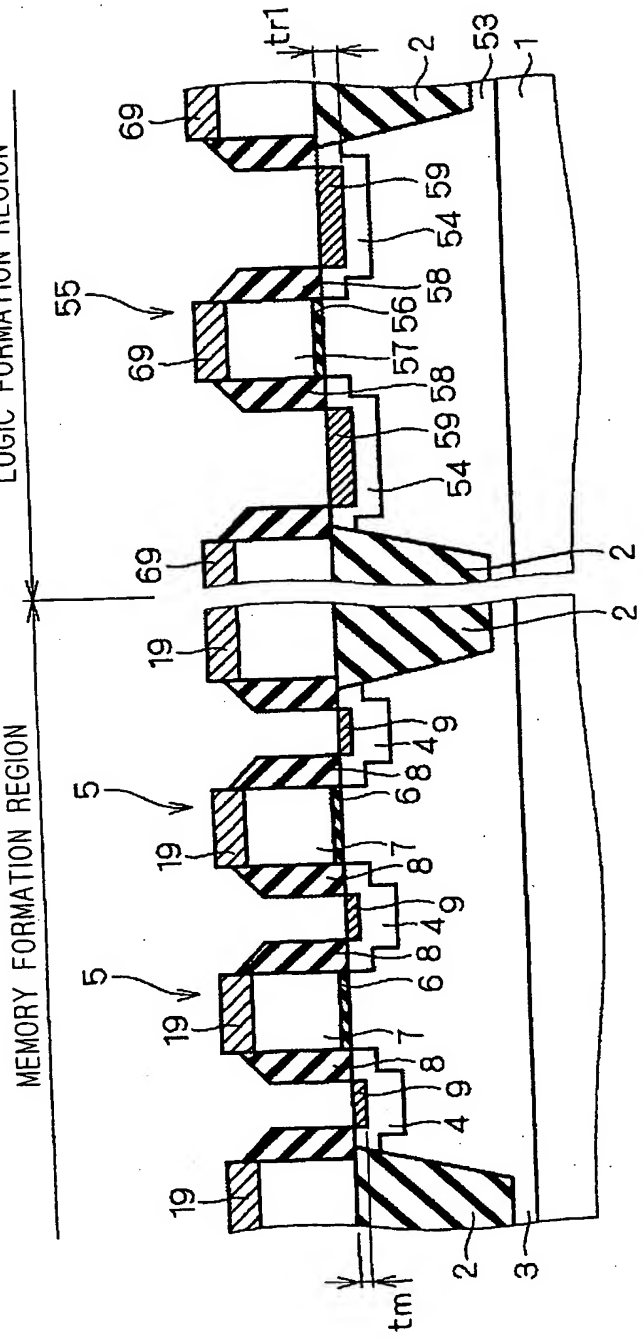
【Fig. 4】


LOGIC FORMATION REGION
MEMORY FORMATION REGION
55
58
54a
54b
54
56
57
53
1
2
dr1
5
8
4a
4b
4
6
7
dm
h
3

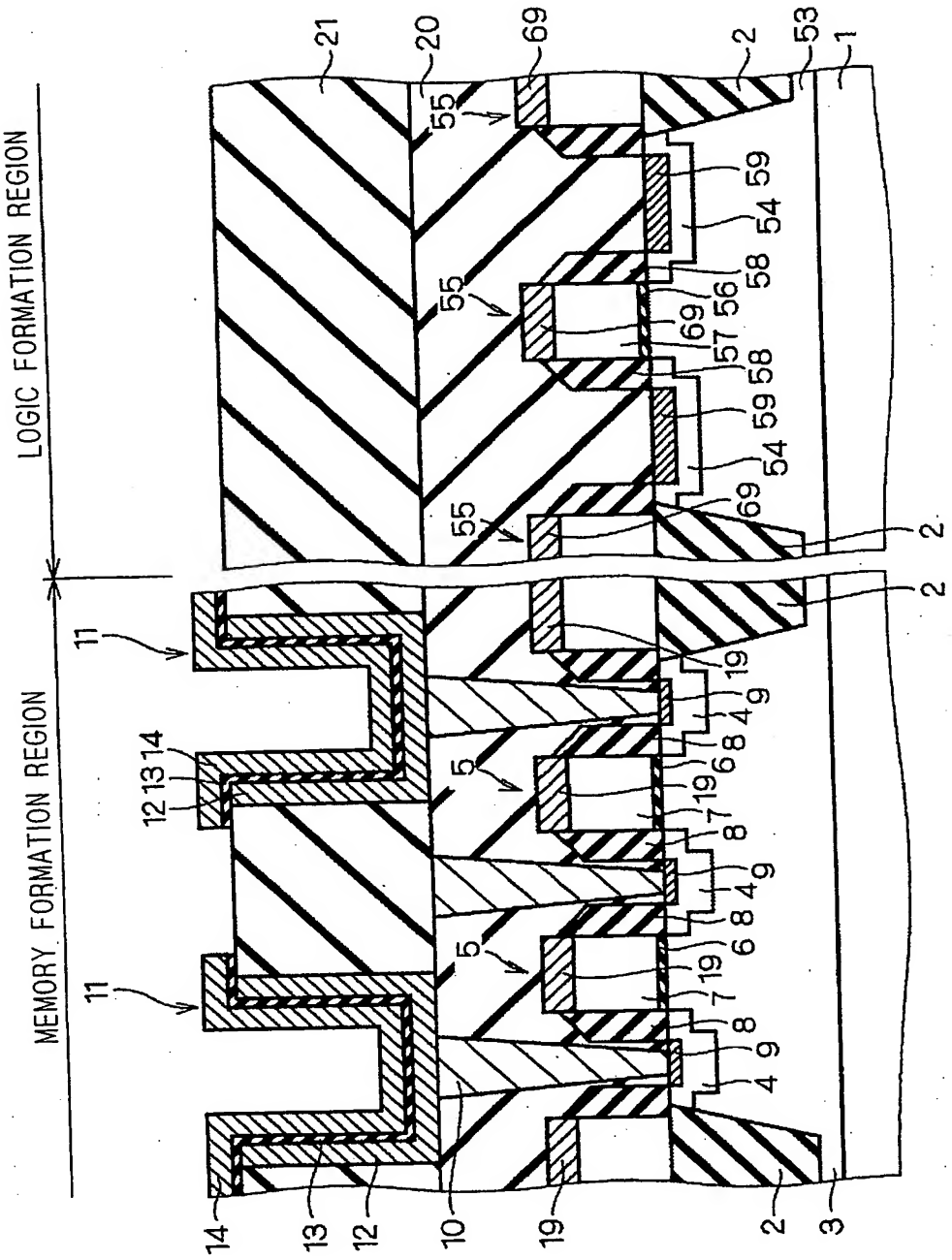
【Fig. 5】


LOGIC FORMATION REGION
MEMORY FORMATION REGION
25 : METAL MATERIAL
tmr1
tmm
25
53
1
2
3
4
5
54
55
56
57
58
6
7
8

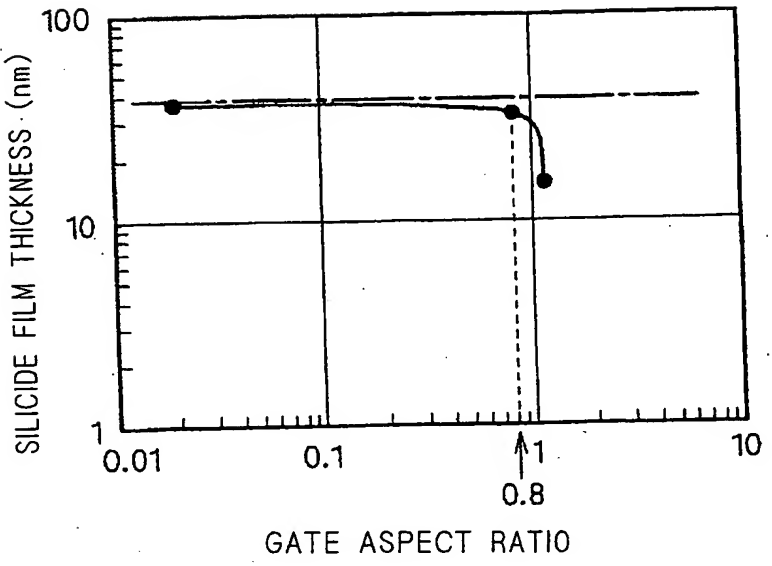
【Fig. 6】


LOGIC FORMATION REGION
MEMORY FORMATION REGION
tr1
tm
1
2
3
4
5
6
7
8
9
19
53
54
55
56
57
58
59
69

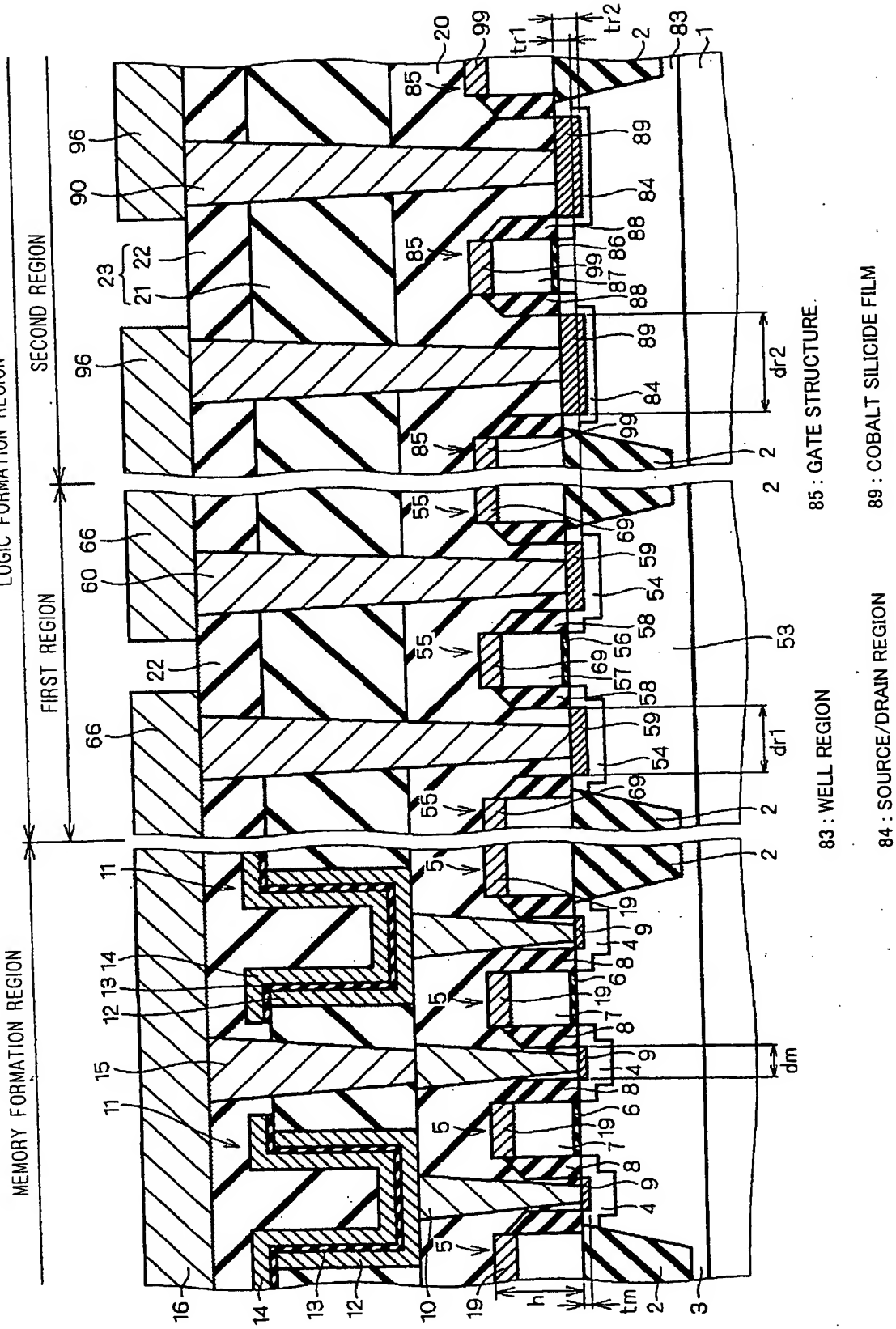
【Fig. 7】


LOGIC FORMATION REGION
MEMORY FORMATION REGION
21
20
69
2
53
1
55
59
54
58
56
57
11
12
13
14
5
19
7
8
6
4
9
10
3

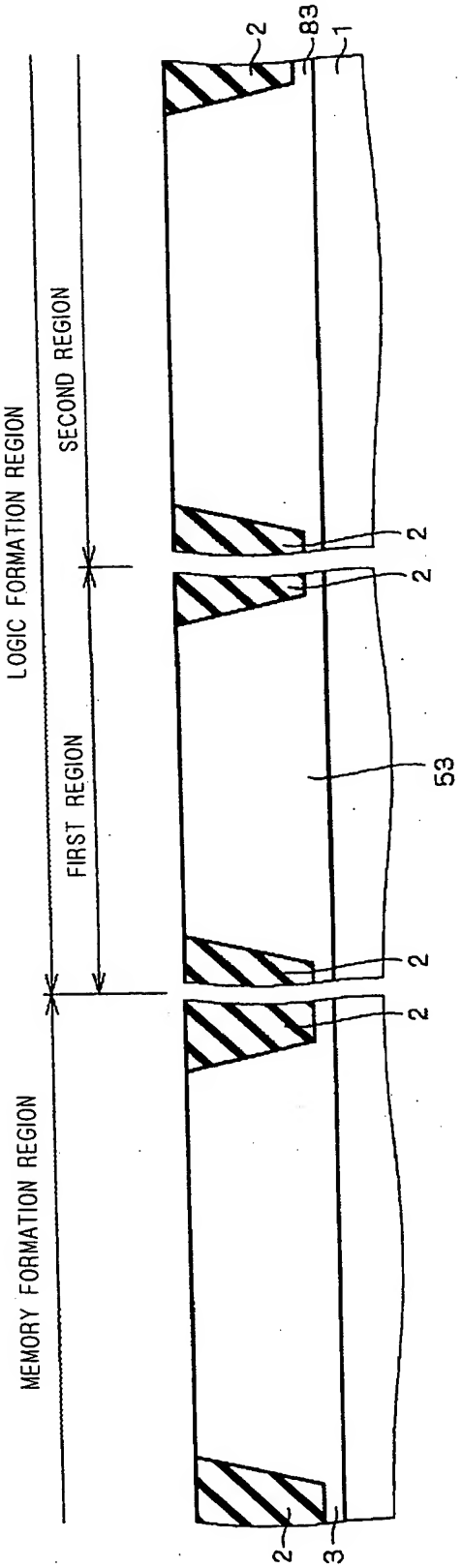
【Fig. 8】


100
10
1
SILICIDE FILM THICKNESS (nm)
0.01
0.1
1
10
0.8
GATE ASPECT RATIO

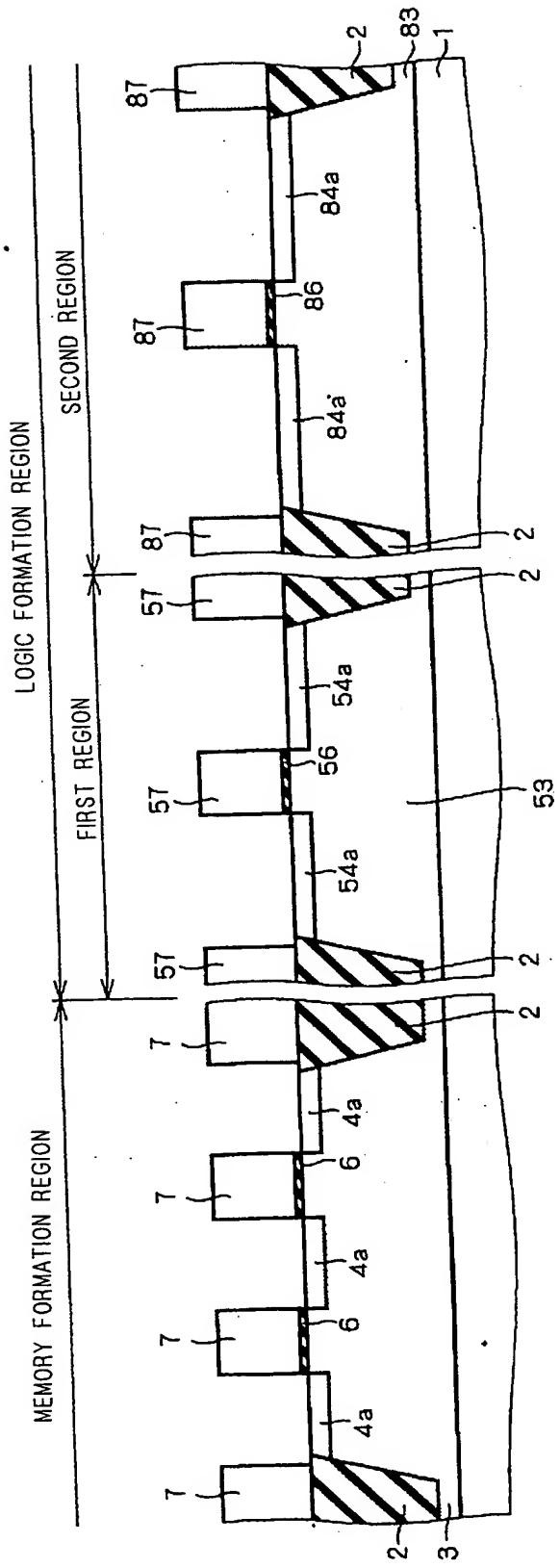
【Fig. 9】


LOGIC FORMATION REGION
SECOND REGION
FIRST REGION
MEMORY FORMATION REGION
dr2
dr1
dm
h
tm
tr1
tr2
85 : GATE STRUCTURE
83 : WELL REGION
84 : SOURCE/DRAIN REGION
89 : COBALT SILICIDE FILM

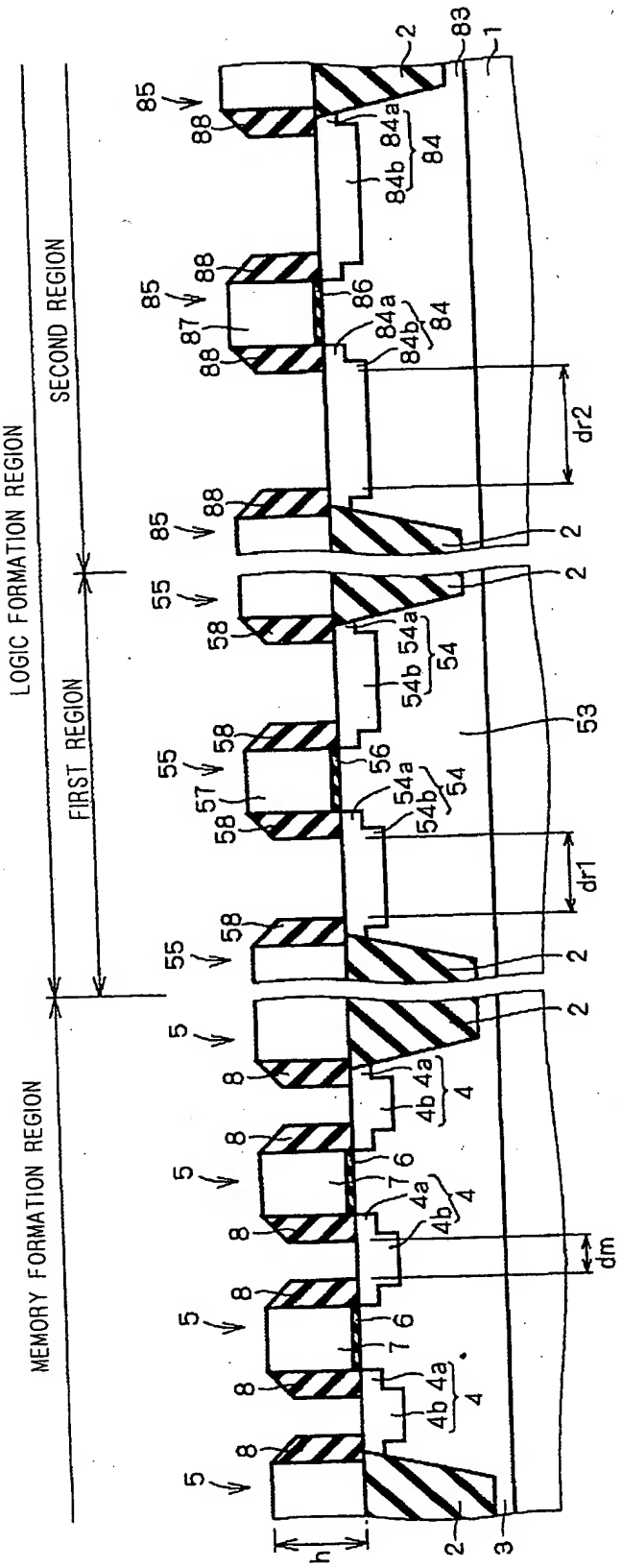
【Fig.1 0】


LOGIC FORMATION REGION
SECOND REGION
FIRST REGION
MEMORY FORMATION REGION
2
83
1
2
2
53
2
2
2
3

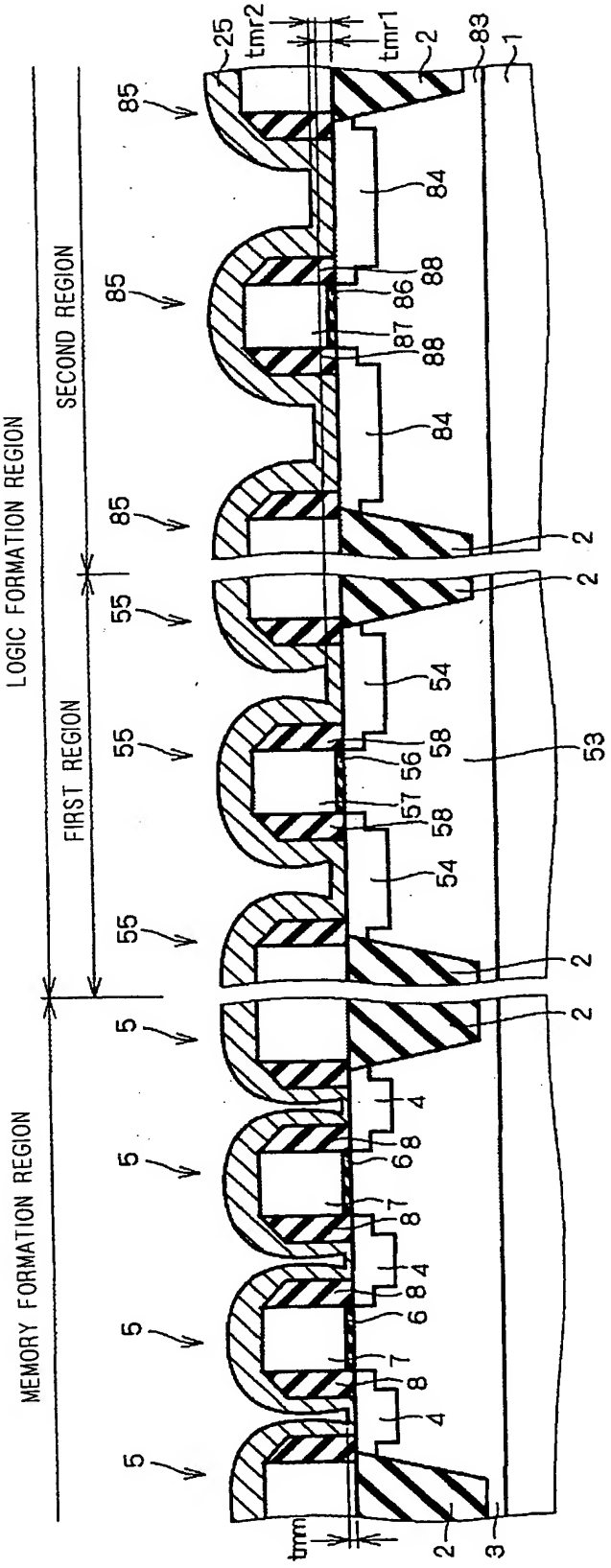
【Fig. 11】


LOGIC FORMATION REGION
SECOND REGION
FIRST REGION
MEMORY FORMATION REGION
87
84a
86
84a
87
87
83
1
2
2
57
54a
56
57
53
54a
57
2
2
7
4a
6
7
4a
6
7
4a
7
2
3

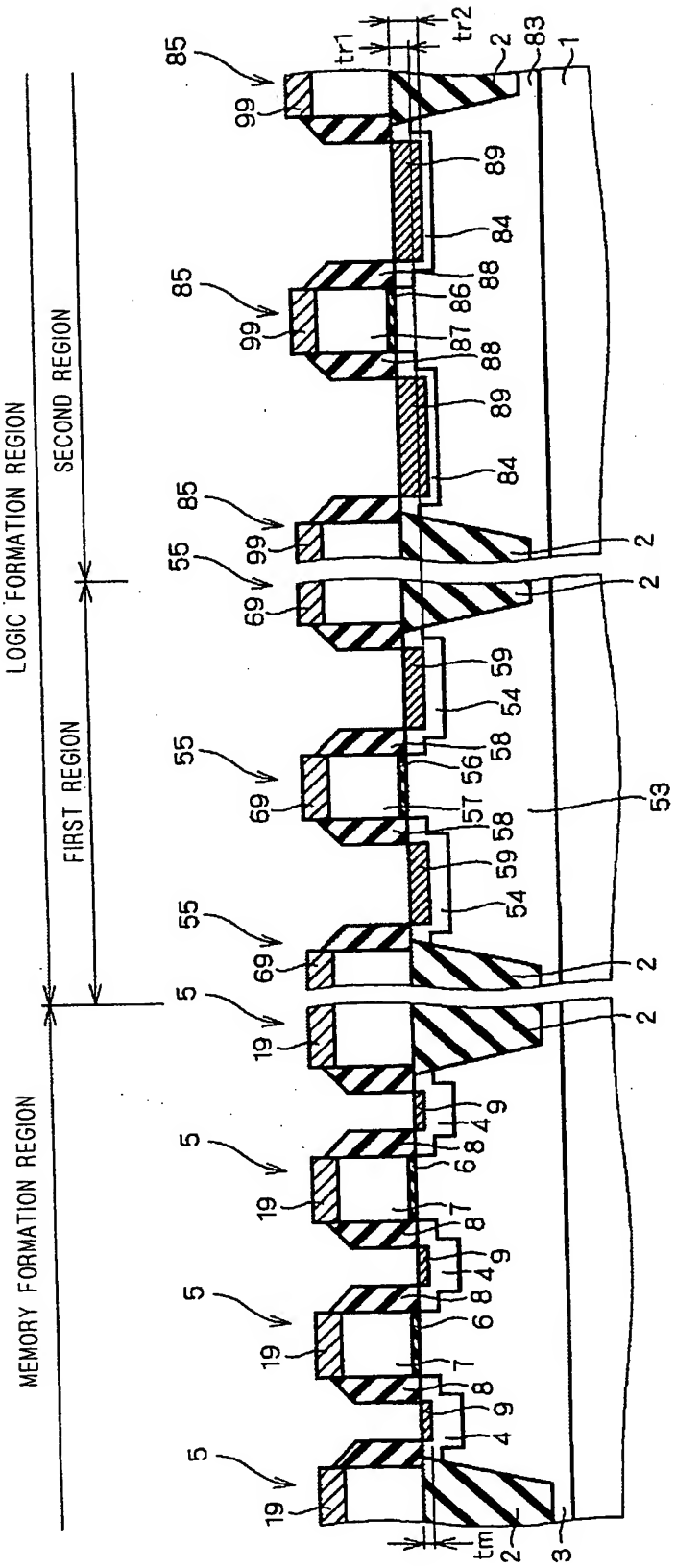
【Fig. 12】


LOGIC FORMATION REGION
SECOND REGION
FIRST REGION
MEMORY FORMATION REGION
dr2
dr1
dm
h

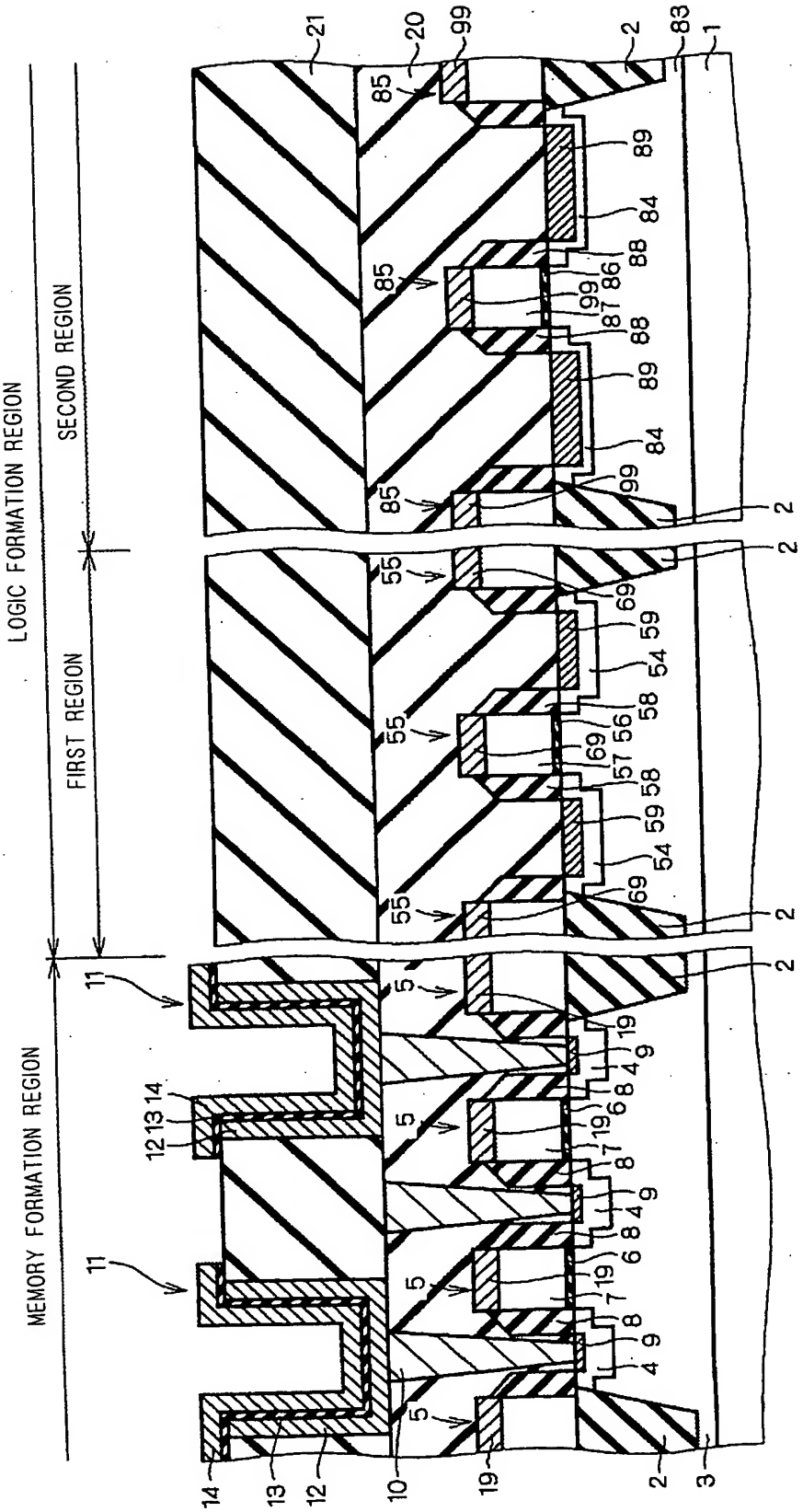
【Fig. 13】


LOGIC FORMATION REGION
SECOND REGION
FIRST REGION
MEMORY FORMATION REGION
tmr2
tmr1
tmm

【Fig. 14】


LOGIC FORMATION REGION
SECOND REGION
FIRST REGION
MEMORY FORMATION REGION
tr1
tr2
tm

【Fig. 15】


LOGIC FORMATION REGION
SECOND REGION
FIRST REGION
MEMORY FORMATION REGION